# SDD Review Document

## Summary

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| --- | --- |
| **Date** | 06/09/21 |
| **Effort** | 20 min |
| **Room/Location** | Virtual |
| **Review Status** | Open |
| **Review name** | SDD\_ADC.doc |
| **Method** | WT, DC, II |
| **Release** | 1.0 |
| **Responsible** | Vicente Guerrero |
| **Project** | Door Control Module |
| **Reason of Review** | Software Design Document Review |

## Comment List

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| --- | --- | --- | --- | --- | --- |
| **No.** | **Reference** | **Comments / Actions** | **Classification (E)rror/Risk / (R)emark** | **Responsible person/Planned date for completion** | **Completion(Name/Date)** |
| 1 | SDD\_ADC.doc/Section 2 | There are some abbreviations such as ADC that are not added. “Antipinch” concept is not defined | Remark | Efren del Real, 06/09/21 |  |
| 2 | SDD\_ADC.doc/Section 4 & 5 | These sections are not explained | Remark | Efren del Real, 06/09/21 |  |
| 3 | Activity diagrams | Activity diagrams do not include a description. | Remark | Efren del Real, 06/09/21 |  |
| 4 |  |  |  |  |  |
| 5 |  |  |  |  |  |
| 6 |  |  |  |  |  |
| … |  |  |  |  |  |

## Check List

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| --- | --- | --- | --- | --- | --- |
| No | Description | OK / NOK / NR | Comment | Responsible person /  Planned date for completion | Status |
| 1 | Does the design comply to the SW architecture? (interfaces, scheduling...) | OK | Design does consider the SWA | Efren del Real, 06/09/21 | Close |
| 2 | Are all requirements allocated to Desing elements? | OK | Requiriments are allocated properly | Efren del Real, 06/09/21 | Close |
| 3 | Are all operations described in an adequate detail and with the adequate notation? | Ok | There are diagrams that express the behaviour | Efren del Real, 06/09/21 | Close |
| 4 | Is the coupling level between SW parts (internal or externals) reduced to the minimum?  Is the justification of all global data written in the design document? | NOK | There are not references to other components | Efren del Real, 06/09/21 | Open |
| 5 | Is each data owned by one unit?  If a data is public (for read and/or for write operations), is its access made using a method provided by the owner?  (if a method is provided for read and write operations on the same pubilc data, the data has to be private) | Ok | External keyword is used | Efren del Real, 06/09/21 | Close |
| 6 | How are the variables initialized? If not initialized, is the reason explained? | NR | Variables are not defined, just functions. | Efren del Real, 06/09/21 | Open |
| 7 | Is the mechanism to initialise the functionality (when needed) described?  (eg: function calls, data acquisition …) | OK | Init function added | Efren del Real, 06/09/21 | Close |
| 8 | In case of global variable (shared or not shared) used in reentrance function (reentrance raised by an ISR), is there a mechanism to avoid data modification during its treatment? | NR | Global variables are not considered | Efren del Real, 06/09/21 | Open |
| 9 | Are Tasks, ISRs and event notification function kept as short as possible? | OK |  | Efren del Real, 06/09/21 | Close |
| 10 | Is the state variable only used in one single module?  (If the state variable needs to be visible from another module (to be avoided), indicate it in the design and use the mechanism of read copy on that variable). | NOK | State variables are not mentioned | Efren del Real, 06/09/21 | Open |
| 11 | Is the event memorization (ex: flag) consumed at the end of each reccurence of a state machine?  Otherwise, the risk is to use an obsolete event (ex: event memorization consumption conditionned by a state transition). | NR |  | Efren del Real, 06/09/21 | Open |
| 12 | In case of asynchronous reception of the same event by several objects (ex: state machine, C function called periodicly…), has each object its own memorization mechanism (ex: separate flags). | NR |  | Efren del Real, 06/09/21 | Open |